Exhibit R-2, RDT&E Budget Item Justification: PB 2013 Defense Advanced Research Projects Agency										DATE: February 2012	
APPROPRIATION/BUDGET ACTIVITY 0400: *Research, Development, Test & Evaluation, Defense-Wide* BA 2: *Applied Research*				R-1 ITEM NOMENCLATURE PE 0602716E: *ELECTRONICS TECHNOLOGY*							
COST ($ in Millions)	**FY 2011**	**FY 2012**	**FY 2013 Base**	**FY 2013 OCO**	**FY 2013 Total**	**FY 2014**	**FY 2015**	**FY 2016**	**FY 2017**	**Cost To Complete**	**Total Cost**
Total Program Element	256.631	215.178	222.416	-	222.416	222.218	246.630	277.900	257.534	Continuing	Continuing
ELT-01: *ELECTRONICS TECHNOLOGY*	256.631	215.178	222.416	-	222.416	222.218	246.630	277.900	257.534	Continuing	Continuing

A. Mission Description and Budget Item Justification

This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices.

This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

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B. Program Change Summary ($ in Millions)	FY 2011	FY 2012	FY 2013 Base	FY 2013 OCO	FY 2013 Total
Previous President's Budget	286.936	215.178	204.416	-	204.416
Current President's Budget	256.631	215.178	222.416	-	222.416
Total Adjustments	-30.305	-	18.000	-	18.000
• Congressional General Reductions	-1.357	-			
• Congressional Directed Reductions	-20.000	-			
• Congressional Rescissions	-1.715	-			
• Congressional Adds	-	-			
• Congressional Directed Transfers	-	-			
• Reprogrammings	-0.363	-			
• SBIR/STTR Transfer	-6.870	-			
• TotalOtherAdjustments	-	-	18.000	-	18.000

Change Summary Explanation

FY 2011: Decrease reflects reductions for the Section 8117 Economic Adjustment, excessive growth, internal below threshold reprogrammings, rescissions and the SBIR/STTR transfer.

FY 2013: Increase reflects minor repricing.

C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
Title: Quantum Information Science (QIS)	7.141	4.700	2.350

Description: The Quantum Information Science (QIS) program will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. Expected applications include: new improved forms of highly secure communication; faster algorithms for optimization in logistics and wargaming; highly precise measurements of time and position on the earth and in space; and new image and signal processing methods for target tracking. Technical challenges include: loss of information due to quantum decoherence; limited communication distance due to signal attenuation; limited selection of algorithms and protocols; and larger numbers of bits. Error correction codes, fault tolerant schemes, and longer decoherence times will address the loss of information. Signal attenuation will be overcome by exploiting quantum repeaters. New algorithm techniques and complexity analysis will increase the selection of algorithms, as will a focus on signal processing. The QIS program is a broad-based effort that will continue to explore the fundamental open questions, the discovery of novel algorithms, and the theoretical and experimental limitations of quantum processing as well as the construction of efficient implementations.

FY 2011 Accomplishments:

- Demonstrated significant progress towards two-qubit gate operations.

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Validated fully self-consistent full configuration interaction (FCI) simulation code. - Demonstrated novel capacitance-based charge sensing and dispersive readouts. - Conducted theoretical analysis of improvement in decoherence time resulting from dynamical decoupling schemes. ***FY 2012 Plans:*** - Explore novel materials, noise characteristics and decoherence mitigation strategies for qubits. - Develop novel intermediate-distance communication of quantum information. - Perform detailed theoretical modeling of single and double qubits. ***FY 2013 Plans:*** - Perform advanced state tomography on qubits. - Demonstrate interconversion of quantum information between different qubits technologies. - Demonstrate transport of quantum information over microscopic scales.			
Title: Terahertz Electronics	19.085	16.413	17.250
Description: Terahertz Electronics will develop the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits for electronics operating in the THz regime and multiple new applications in imaging, radar, communications, and spectroscopy. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules. ***FY 2011 Accomplishments:*** - Demonstrated high performance fully integrated transmit and receive circuits at 0.67 THz. - Demonstrated solid state exciters and Terahertz High Power Amplifier modules at 0.67 THz. - Demonstrated key integration and metrology technologies required for microsystems utilizing 0.67 THz active device and integrated circuits. ***FY 2012 Plans:*** - Continue the development of device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Develop key device, integration, and metrology technologies to enable the manufacture of microsystems, such as heterodyne detectors, between 0.67 and 1.03 THz for advanced communications and radar applications at sub-millimeter wave frequencies. ***FY 2013 Plans:*** - Achieve key device and integration technologies to realize compact, high performance electronic circuits operating beyond 1.03 THz.			
Title: High Frequency Integrated Vacuum Electronic (HiFIVE) ***Description:*** The objective of the High Frequency Integrated Vacuum Electronics (HiFIVE) program is to develop and demonstrate new high-performance and low-cost technologies for implementing high-power millimeter-wave sources and components. This program is developing new semiconductor and micro-fabrication technologies to produce vacuum electronic high-power amplifiers for use in high-bandwidth, high-power transmitters. Innovations in design and fabrication are being pursued to enable precision etching, deposition, and pattern transfer techniques to produce resonant cavities, electrodes, and magnetics, and electron emitting cathodes for compact high-performance millimeter wave devices. These new technologies will eliminate the limitations associated with the conventional methods for assembly of high-power sources in this frequency range. ***FY 2011 Accomplishments:*** - Completed advanced cathode development activities. - Initiated fabrication and initial testing of a high-power amplifier prototype device incorporating HiFIVE micro-fabrication technologies into a compact module form factor. - Demonstrated 220 Gigahertz (GHz) solid state driver amplifier technology for implementations as exciter circuits for high power amplifiers. ***FY 2012 Plans:*** - Continue fabrication and initial testing of a high-power amplifier prototype device incorporating HiFIVE micro-fabrication technologies into a compact module form factor. - Continue efforts to perform laboratory measurements of performance and validate RF power levels. - Initiate integration of compact amplifier technology at G-band in a miniaturized tube form factor. ***FY 2013 Plans:*** - Demonstrate integrated and compact amplifier technology at G-band in a tube form factor. - Complete laboratory measurements of performance of miniaturized tube amplifier at 220GHz.	7.511	5.000	5.000
Title: Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) ***Description:*** The vision of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program is the development of biological-scale neuromorphic electronic systems for autonomous, unmanned, robotic systems where humans are	23.706	29.555	24.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013

currently the only viable option. The successful development of this technology will revolutionize warfare by providing intelligent terrestrial, underwater, and airborne systems that remove humans from dangerous environments and remove the limitations associated with today's remote-controlled robotic systems. Applications for neuromorphic electronics include not only robotic systems, but also natural human-machine interfaces and diverse sensory and information integration applications in the defense and civilian sectors. If successful, the program will also reinvigorate the maturing microelectronics industry by enabling a plethora of computer and consumer electronics applications.

FY 2011 Accomplishments:

- Demonstrated all core microcircuit functions in hybrid complementary metal-oxide semiconductor (CMOS) electronic synapse hardware.
- Demonstrated a dynamic neural system simulation of approximately 1 million neurons that shows plasticity, self-organization, and network stability in response to sensory stimulus and system level reinforcement.
- Developed tools to design electronic neuromorphic systems of 100 billion neurons with mammalian connectivity.
- Demonstrated virtual environments with a selectable range of complexity to train and test systems.
- Specified large-scale system architecture and a chip fabrication process supporting 1 million neurons per square centimeter and 10 billion synapses per square centimeter.

FY 2012 Plans:

- Design and simulate in software a complete neural system of ~10 billion synapses and ~1 million neurons performing cognitive tasks in a virtual environment comparable to those routinely tested in mice.
- Design and validate a hardware neural system of ~10 billion synapses and ~1 million neurons.
- Demonstrate a chip fabrication process and development plan supporting ~10 billion synapses per square centimeter and ~1 million neurons per square centimeter.
- Downselect among fabrication processes for CMOS and novel synaptic memory to optimize for density and power performance.
- Refine design tools and techniques by codifying design rules and component properties and matching them to fabrication and simulation capabilities.
- Demonstrate a virtual environment supporting visual perception, decision and planning, and navigation environments fully integrated with software or hardware neural systems enabling the testing, training, and evaluation of these neural systems.
- Introduce modalities of competition within the virtual environment to further tailor the evolution of the neural systems.

FY 2013 Plans:

- Demonstrate fabricated neuromorphic chips of 1 million neurons performing behavioral tests in the virtual environment.
- Fabricate additional neuromorphic chips of 1 million neurons with more advanced communication, processing, and learning capacity.
- Design an initial multi-chip neuromorphic system of approximately 100 million neurons.

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Perform animal experiments to quantify neuronal activity in sensory, navigation, and motor brain regions. - Expand the feature set of the virtual environment to include auditory perception and proprioception. - Utilize DoD-relevant platforms such as small UAVs to demonstrate capabilities of developed systems in real environments. - Demonstrate scalability of hardware systems and future densities and power consumption for next-generation systems.			
Title: Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) ***Description:*** The objective of the Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) program is to develop chip-scale dense waveguide modular technology to achieve true embedded phase array control for beams equivalent to 10W average power, less than 0.1 degree instantaneous field of view (IFOV), greater than 45 degree total field of view (TFOV), and frame rates of greater than 100 hertz (Hz) in packages that are "chip-scale." Such performance will represent a three order of magnitude increase in speed, while also achieving a greater than two orders of magnitude reduction in size. Additionally, the integrated phase control will provide the unprecedented ability to rapidly change the number of simultaneous beams, beam profile, and power-per-beam, thus opening a whole new direction in operational capability. Key technical challenges include the ability to achieve the needed facet density (facet pitch should be on the order of a wavelength or two), control the relative phase across all facets equivalent to 9-bits, and efficiently couple and distribute coherent light to facets from a master laser oscillator with an integrated waveguide structure. Related projects and studies have pointed to the significant system-level pay-offs of the new proposed technology. ***FY 2011 Accomplishments:*** - Demonstrated phase locking of multiple individual emitters (vertical cavity surface emitting lasers) to single master source on a single integrated chip - Demonstrated chip scale beam-forming and steering capability in laboratory with a 20°x14° scan window using 16 elements. ***FY 2012 Plans:*** - Demonstrate 8x8 integrated photonic chip scale array beam forming with path towards a 32x32 array. - Demonstrate 10°x10° beam steering with <20dB sidelobes.	7.334	7.466	-
Title: Electric Field Detector (E-FED) ***Description:*** The goal of the Electric Field Detector (E-FED) program is to develop a small, room-temperature electric field sensor/sensor array based on new optical electric field sensor architectures. Electric fields are ubiquitous in the warfighter environment. It is expected that these compact sensor arrays will be potentially useful for the monitoring of brain activity and muscle action without the need to apply electrodes directly in or on the surface of the skin. The arrays would also be useful for the remote sensing of electronics, motors, and communications devices enabling the sensing of these devices at greater distances with a more unobtrusive and portable system.	2.795	2.304	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
FY 2011 Accomplishments: - Demonstrated electric field sensors sensitive to an alternating electric field of 1 millivolt (mV)/meter root hertz from 1-10,000 hertz (Hz). - Developed techniques to increase the frequency range, dynamic range and sensitivity of the electric field sensors while reducing their size. ***FY 2012 Plans:*** - Demonstrate a sensor array with at least 25 elements with high sensitivity to an alternating electric field for source localization. - Demonstrate sensors sensitive to an alternating electric field of 1 microvolt (μV)/meter root hertz from 0.5-1,000,000 hertz (Hz), sufficient for brain activity monitoring.			
Title: Self-HEALing mixed-signal Integrated Circuits (HEALICs)	10.740	15.330	6.190
Description: The goal of the Self-HEALing mixed-signal Integrated Circuits (HEALICs) program is to develop technologies to autonomously maximize the number of fully operational mixed-signal systems-on-a-chip (SoC) per wafer that meet all performance goals in the presence of extreme process technology variations, environmental conditions, and aging. Virtually all DoD systems employ mixed-signal circuits for functions such as communications, radar, navigation, sensing, high-speed image and video processing. A self-healing integrated circuit is defined as a design that is able to sense undesired circuit/system behaviors and correct them automatically. As semiconductor process technologies are being scaled to even smaller transistor dimensions, there is a dramatic increase in intra-wafer and inter-die process variations, which have a direct impact on realized circuit performance, as well as significantly increased sensitivity to temperature and ageing effects. This applied research program aims to develop techniques to regain lost performance and stabilize operation of mixed-signal SoCs over system lifetimes. Consequently, the long-term reliability of DoD electronic systems is expected to be significantly enhanced. ***FY 2011 Accomplishments:*** - Continued development of self-healing mixed-signal cores. - Demonstrated significant increase in performance yield of mixed-signal cores, including a 1.8 GHz input Sigma Delta analog to digital converter (ADC) for element-level digital phased-array radar, a 60 GHz communications transceiver, and a 1 giga-samples per second time-interleaved ADC for an electronic warfare receiver, to greater than seventy-five percent with minimal power and die area overhead. - Development of a self-healing IP core library for DoD user access. ***FY 2012 Plans:*** - Integrate previously demonstrated mixed-signal cores into a full self-healing microsystems/SoCs.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Develop global self-healing control at the microsystem/SoC level. - Demonstrate simulated increase in performance yield of mixed-signal SoCs to greater than ninety-five percent with minimal power and die area overhead. - Continue development of self-healing IP core library for DoD user access and demonstrate self-healing integrated circuit designs leveraging cores from multiple performer teams. ***FY 2013 Plans:*** - Demonstrate increase in performance yield of fabricated mixed-signal SoCs to greater than ninety-five percent with minimal power and die area overhead. - Make self-healing IP core library widely available for DoD user access.			
Title: Efficient Linearized All-Silicon Transmitter ICs (ELASTx)	5.491	4.806	4.272
Description: The goal of the Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program is the development of revolutionary high-power/high-efficiency/high-linearity single-chip millimeter (mm)-wave transmitter integrated circuits (ICs) in leading edge silicon technologies for future miniaturized communications and sensor systems on mobile platforms. The high levels of integration possible in silicon technologies enable on-chip linearization, complex waveform synthesis, and digital calibration and correction. Military applications include ultra-miniaturized transceivers for satellite communications-on-the-move, collision avoidance radars for micro-/nano-air vehicles, and ultra-miniature seekers for small munitions. The technology developed under this program could also be leveraged to improve the performance of high-power amplifiers based-on other nonsilicon technologies through heterogeneous integration strategies. Significant technical obstacles to be overcome include the development of highly efficient circuits for increasing achievable output power of silicon devices (e.g., device stacking, power combining) at mm-waves; scaling high-efficiency amplifier classes to the mm-wave regime; integrated linearization architectures for complex modulated waveforms; and robust RF/mixed-signal isolation strategies. ***FY 2011 Accomplishments:*** - Continued development of watt-level, high power added efficiency (PAE) silicon-based power amplifier (PA) circuits at Q-band frequencies. - Continued development of linearized transmitter circuits based on high PAE PAs at Q-band frequencies. - Initiated development of watt-level, high PAE silicon-based PA circuits at W-band frequencies. - Initiated development of linearized transmitter circuits based on high PAE PAs at W-band frequencies. - Continued development of on-wafer calibration techniques for deeply scaled silicon transistors, and measurement techniques for mm-wave linearized transmitter circuits with complex modulated waveforms. ***FY 2012 Plans:*** - Demonstrate watt-level, high PAE silicon-based PA circuits at Q-band frequencies.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Demonstrate linearized transmitter circuits based on high PAE PAs at Q-band frequencies with complex modulated waveforms. - Continue development of watt-level, high PAE silicon-based PA circuits at W-band frequencies. - Continue development of linearized transmitter circuits based on high PAE PAs at W-band frequencies. ***FY 2013 Plans:*** - Demonstrate watt-level, high PAE silicon-based PA circuits at W-band frequencies. - Demonstrate linearized transmitter circuits based on high PAE PAs at W-band frequencies with complex modulated waveforms. - Initiate development of watt-level, high PAE silicon-based PA circuits at D-band frequencies. - Initiate development of linearized transmitter circuits based on high PAE PAs at D-band frequencies.			
Title: Compact Mid-Ultraviolet Technology ***Description:*** The goal of the Compact Mid-Ultraviolet Technology program is to develop compact high-brightness Middle Ultraviolet source and detector technologies based on wide band gap diode structures. This program will address a critical technology shortfall preventing mid-UV capability in portable chem-bio defense systems for aerosol detection (enhanced capability for small particulates), chem-bio identification (Raman scattering and spectroscopy), and chemical decontamination/water purification applications. The technologies will also address solar-blind detectors for missile plume identification. ***FY 2011 Accomplishments:*** - Continued development for large non-absorbing (UV transparent) low-defect-density substrate materials on which to grow devices. - Continued high-quality, highly-strained epitaxy developments to confine carriers and provide the required energy band offsets. - Increased electric injection of carriers to improve quantum efficiency of light-emitting diodes. - Continued the development of low-resistance non-absorbing contacts. - Demonstrated first optically pumped semiconductor mid-UV laser below 250 nm wavelength. ***FY 2012 Plans:*** - Demonstrate diode operation at proposed mid-UV wavelength over a broader range of operating conditions. - Increase the diameter of high-quality aluminum nitride substrates and ternary templates to enable development of optimized devices. - Demonstrate high wall plug efficiency, high brightness Light-emitting Diode (LED) operating between 250-270nm. - Demonstrate 5mW semiconductor lasers operating below 250nm in wavelength. - Design system insertions utilizing highly-efficient UV LEDs for advanced detection capability.	16.013	14.189	-
Title: Adaptive Radio Frequency Technology (ART)	14.068	21.918	25.082

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013

Description: There is a critical ongoing military need for flexible, affordable, hand-held cognitive military communications systems. The Adaptive Radio Frequency Technology (ART) program will provide the warfighter with a new, fully adaptive radio platform capable of sensing the electromagnetic and waveform environment in which it operates, making decisions on how to best communicate in that environment, and rapidly adapting its hardware to meet ever-changing requirements, while simultaneously significantly reducing the size, weight and power (SWaP) of such radio nodes. ART will also equip each warfighter, as well as small-scale unmanned platforms, with compact and efficient signal identification capabilities for next-generation cognitive communications, sensing and electronic warfare applications. ART technology will also enable rapid radio platform deployment for new waveforms and changing operational requirements. ART aggregates the Feedback Linearized Microwave Amplifiers program, the Analog Spectral Processing program, and Chip Scale Spectrum Analyzers (CSSA) program, and initiates new thrusts in Cognitive Low-energy Signal Analysis and Sensing Integrated Circuits (CLASIC), RF Field-Programmable Arrays (RF-FPGA), and Dynamic Live Active Nulling (DyLAN).

FY 2011 Accomplishments:

- Continued development of feedback-linearized InP Heterojunction Bipolar Transistor (HBT) monolithic low-noise amplifiers with improved third-order-intercept point and noise figure for potential transition to signal intelligence and electronic warfare platform applications.
- Continued development of feedback linearized amplifier approaches to analog/RF applications such as high-speed/high dynamic range sample-and-holds and active impedance matching of electrically small antennas, and development of an integrated field-effect-transistor switch process in support of these applications.
- Demonstrated miniaturized, low-loss, tunable and reconfigurable RF, intermediate frequency, and sensor filter banks and continued to explore potential transition opportunities to various military communications and sensing systems.
- Continued development of ultra-high (1e5 at 3 GHz) quality-factor micro-electromechanical resonators for potential use in an RF channelizer for fast spectrum sensing in cognitive radios.
- Initiated development of novel signal recognition sensor integrated circuits that can achieve >400 times reduction in signal recognition energy as compared to state of the art sensor systems.

FY 2012 Plans:

- Complete development of feedback-linearized InP HBT monolithic low-noise amplifiers with improved third-order-intercept point and noise figure for potential transition to signal intelligence and electronic warfare platform applications.
- Complete development of feedback linearized amplifier approaches to analog/RF applications such as high-speed/high dynamic range sample-and-holds and active impedance matching of electrically small antennas, and development of an integrated field-effect-transistor switch process in support of these applications.
- Continue development of novel signal recognition sensor integrated circuits that can achieve >400 times reduction in signal recognition energy as compared to state of the art sensor systems.

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Initiate development of reconfigurable RF circuit (RF FPGA) technologies. - Initiate development of RF signal cancellation concepts which will actively eliminate unwanted signals within a receiver. ***FY 2013 Plans:*** - Continue development of novel signal recognition sensor integrated circuits. - Continue development of reconfigurable RF circuit (RF FPGA) technologies. - Continue development of integrated cancellation circuits for the purpose of RF filter replacement in low-SWaP military radios and signal intelligence platforms.			
Title: Nitride Electronic NeXt-Generation Technology (NEXT) ***Description:*** The objective of the Nitride Electronic NeXt-Generation Technology (NEXT) program is to develop a revolutionary nitride transistor technology that simultaneously provides extremely high-speed and high-voltage swing [Johnson Figure of Merit (JFoM) larger than 5 THz-V] in a process consistent with large scale integration in enhancement/depletion (E/D) mode logic circuits of 1000 or more transistors. In addition, this fabrication process will be manufacturable, high-yield, high-uniformity, and highly reliable. The accomplishment of this goal will be validated through the demonstration of specific Program Process Control Monitor (PCM) Test Circuits such as 5, 51, and 501-stage of ring oscillators in each program phase. ***FY 2011 Accomplishments:*** - Developed high-performance Gallium Nitride Field Effect Transistors (FETs) with cutoff frequencies above 350GHz. - Achieved yield required for modest integration levels of E/D mode mixed signal circuits. - Demonstrated self-aligned structure with short gate length, novel barrier layers and reduced parasitic effects. - Developed an optimized enhancement mode power switch process to complement high frequency FET process. ***FY 2012 Plans:*** - Continue scaling efforts for self-aligned structures with short gate length, novel barrier layers and reduced parasitic elements to achieve additional cutoff frequency performance gains. - Continue transistor performance trade-space analysis to achieve ultra-fast power switching capability. - Continue development of an optimized enhancement mode power switch process to complement high frequency FET process. - Establish an integrated process for power switching and Microwave Monolithic Integrated Circuit (MMIC) capability using advanced wide band gap devices. - Increase passive element performance of MMIC process utilizing both enhancement and depletion mode devices. - Initiate development of complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes. ***FY 2013 Plans:***	12.217	13.130	11.560

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Continue development of complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes. - Demonstrate monolithic integration of mixed signal and power amplifier circuits.			
Title: Non-Volatile Logic ***Description:*** The objective of the Non-Volatile Logic program was to develop the theory, design, and fabrication methodology, and demonstrate example circuits that utilize new computational state variables. The program fabricated and demonstrated circuits that dissipate lower power, per logic operation, while having equal or better computational throughput as equivalent charge-based circuits. Non-Volatile Logic is an outgrowth of the Spin Torque Transfer Random Access Memory program. ***FY 2011 Accomplishments:*** - Developed circuits capable of performing logic functions based on the nano-magnetic re-orientation information and not on the movement of electrical charge. - Demonstrated fabrication techniques to make nano-magnetic based logic devices.	5.911	-	-
Title: Photonically Optimized Embedded Microprocessor (POEM) ***Description:*** Current trends in scaling microprocessor performance are projected to saturate and fall far short of future military needs. Microprocessor performance is saturating and leading to reduced computational efficiency because of the limitations of electrical communications. The Photonically Optimized Embedded Microprocessor (POEM) program will demonstrate chip-scale, silicon-photonic technologies that can be integrated within embedded microprocessors for seamless, energy-efficient, high-capacity communications within and between the microprocessor and dynamic random access memory (DRAM). This technology will propel microprocessors onto a higher performance trajectory by overcoming the "memory wall", and thus satisfy projected microprocessor performance needs for memory intensive applications. ***FY 2011 Accomplishments:*** - Demonstrated an optical transceiver (transmitter and receiver), comprised of complementary metal-oxide semiconductor (CMOS)-compatible Si photonic devices and electronic drivers, and operating at 10 gigabits/second, with a world record efficiency of 530 femtojoules per bit of data. The transmitter and receiver each performed with record energy efficiencies of 135 and 395 femtojoules per bit of data, respectively. - Demonstrated a CMOS-compatible, waveguide coupled, high-gain-bandwidth avalanche photodiode operating at 40 gigabits/second with a gain-bandwidth product of 320 gigahertz. ***FY 2012 Plans:*** - Demonstrate an eight wavelength, wavelength-division-multiplexed, CMOS-compatible, optical link with 80 gigabit/second capacity and a link energy efficiency of 970 femtojoules per bit of data.	21.159	26.000	22.417

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Develop DRAM-compatible modulator, multiplexer, coupler, and photodetector devices and associated drivers for low-power, high capacity photonic links. ***FY 2013 Plans:*** - Demonstrate a DRAM-compatible photonic link which enables photonic communication between CMOS and DRAM chips with 80 gigabits/second capacity and a link energy efficiency of 450 femtojoules per bit of data. - Continue to develop and improve CMOS-compatible modulator, multiplexer, coupler, and photodetector devices and associated drivers for low-power, high capacity photonic links for insertion in final demonstration.			
Title: Analog-to-Information (A-to-I) Look-Through*	11.429	11.500	3.800
Description: *Formerly Analog-to-Information (A-to-I) Receiver Development The Analog-to-Information (A-to-I) Look-Through program will fundamentally improve the operational bandwidth, linearity, and efficiency of electronic systems where the objective is to receive and transmit information using electromagnetic (radio) waves under extreme size/weight/power and environmental conditions required for DoD applications. The A-to-I Look-Through program will develop ultra-wideband digital radio frequency (RF) receivers based on Analog-to-Information Converter (AIC) technology. Compared to conventional RF receivers, AIC-based designs will increase receiver dynamic range and frequency band of regard while reducing data glut, power consumption and size. Likewise, limitations of current art power amplifier technology in simultaneously achieving high operational bandwidth, linearity, efficiency and power has resulted in well documented instances of electronic fratricide. This program will overcome these limitations by converting digital signals directly to high power RF analog signals, thus eliminating the traditional high power amplifiers that are limited by the above-mentioned tradeoffs. Transition is anticipated into airborne SIGINT and electronic warfare systems, as well as ground-based special operations forces systems. ***FY 2011 Accomplishments:*** - Completed integration of dual-channel Nyquist Folding A-to-I Receiver prototypes. - Developed and implemented novel algorithms for processing of realistic, Nyquist-folded signal data. - Conducted multiple ground and flight tests of the Nyquist Folding Receiver, detecting and measuring a wide range of signal types in operationally-realistic environments. - Initiated the transmit thrust efforts. ***FY 2012 Plans:*** - Finalize implementation and testing of A-to-I receiver data processing algorithms with focus on improving algorithm robustness against operationally-realistic conditions. - Finalize technology transition plans and transition A-to-I receivers to one or more operationally-focused end user organizations. - Develop and demonstrate through analysis, simulation and measurement suitable Look-Through transmitter architectures.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Design, tape out and characterize in laboratory environment Look-Through transmitter cells and signal combining structures. - Design, tape out and characterize in laboratory environment Look-Through transmitters with high linearity, high power, wide bandwidth and high efficiency. ***FY 2013 Plans:*** - Complete design, tape out and testing of full-scale Look-Through transmitters with focus on insertion into specific DoD systems of interest. - Complete insertion of Look-Through transmitters into DoD systems of interest and demonstrate the transmitter performance in operationally-realistic environments.			
Title: Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE)	7.578	8.000	9.000
Description: The Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) program addresses the passive imaging needs for multi-band, wide field of view (FOV) and high-resolution imaging for ground and near ground platforms. The AWARE program aims to solve the technological barriers that will enable FOV, high resolution and multi-band camera architectures by focusing on four major tasks: high space-bandwidth product (SBP) camera architecture; small pitch pixel focal plane array architecture; broadband focal plane array architecture; and multi-band focal plane array architecture. The AWARE program demonstrates technologies such as detectors, focal plane arrays, read-out integrated circuitry, and computational imaging that enable wide FOV and high space bandwidth, novel optical designs, high resolution and multiple wavelength band imagers. These technologies will be integrated into subsystem demonstrations under the related MT-15 project in PE 0603739E. This program also includes technologies previously addressed in the Wide Field of View (formerly MultiScale Optical Sensor Array Imaging (MOSAIC)) program. ***FY 2011 Accomplishments:*** - Constructed and demonstrated a compact, multiscale, 1.5 Gigapixel snapshot imaging system with a potential capacity of 2.5 Gigapixels. The aperture of the camera is 4 inches with a Field of View (FOV) of 120 x 70 degrees and an achieved resolution of 64 microradians. The volume of the optical system is approximately 3 orders of magnitude smaller than state of the art Gigapixel capable snapshot imagers. - Designed next generation imaging systems with 10 -20 microradians resolution over large fields (120 x 70 degrees). ***FY 2012 Plans:*** - Fabricate the AWARE 10 Gigapixel system with about 20 Gigapixels, including second generation micro-optics and electronics. The key objectives will be to reduce the iFOV by 3X relative to the Phase I camera and achieve a 4X reduction in electronics SWaP. ***FY 2013 Plans:***			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Complete fabrication of the AWARE 50 camera (30 Gigapixels) with 2-3X improvement over AWARE 10 with < 1 cm ground sample distance (GSD) at 1 km. - Complete testing and design studies for a smaller scale microcamera for additional size, weight and power (SWaP) reduction.			
Title: Diverse & Accessible Heterogeneous Integration (DAHI)	13.900	14.772	26.794
Description: Prior DARPA efforts have demonstrated the ability to monolithically integrate inherently different semiconductor types to achieve near-ideal "mix-and-match" capability for DoD circuit designers. Specifically, the Compound Semiconductor Materials On Silicon (COSMOS) program, in which transistors of Indium Phosphide (InP) can be freely mixed with silicon complementary metal-oxide semiconductor (CMOS) circuits to obtain the benefits of both technologies (very high speed and very high circuit complexity/density, respectively). The Diverse & Accessible Heterogeneous Integration (DAHI) effort will take this capability to the next level, ultimately offering the seamless co-integration of a variety of semiconductor devices (for example, Gallium Nitride, Indium Phosphide, Gallium Arsenide, Antimonide Based Compound Semiconductors), microelectromechanical (MEMS) sensors and actuators, photonic devices (e.g., lasers, photo-detectors) and thermal management structures. This capability will revolutionize our ability to build true "systems on a chip" (SoCs) and allow dramatic size, weight and volume reductions for a wide array of system applications. FY 2011 and FY 2012 incorporates the COSMOS program into DAHI. In the Applied Research part of this effort, high performance RF/optoelectronic/mixed-signal SoCs for specific DoD transition applications will be developed as a demonstration of the DAHI technology. In addition, in order to provide maximum benefit to the DoD, as these processes are developed, they will be transferred to a manufacturing flow and made available (with appropriate computer aided design support) to a wide variety of DoD laboratory, FFRDC, academic and industrial designers. Manufacturing yield and reliability of the DAHI technologies will be characterized and enhanced. This program has basic research efforts funded in PE 0601101E, Project ES-01. ***FY 2011 Accomplishments:*** - Continued to optimize compound-semiconductor on silicon process technologies for fine-scale heterogeneous integration in very large-scale integrated circuit with high manufacturing and performance yield. - Continued design and test of advanced mixed-signal circuit demonstrators, specifically heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converters with in situ silicon enabled calibration and linearization. - Initiated a multi-user compound-semiconductor on silicon foundry process which will ultimately be accessible to the wider defense and commercial integrated circuit design community. ***FY 2012 Plans:*** - Complete design and test of advanced heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converters with in situ silicon enabled calibration and linearization.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Initiate design and test of higher complexity heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converters with in situ silicon enabled calibration and linearization. - Continue multi-user compound-semiconductor on silicon foundry process, which will ultimately be accessible to the wider defense and commercial integrated circuit design community. - Develop new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches. - Initiate design of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, optoelectronic RF signal sources, and laser radar and imaging array chips. ***FY 2013 Plans:*** - Optimize new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches. - Initiate manufacturing, yield and reliability enhancement for an expanded multi-user foundry capability based on developed diverse heterogeneous integration processes. - Continue design of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, optoelectronic RF signal sources, and laser radar and imaging array chips.			
Title: Leading Edge Access Program (LEAP) ***Description:*** The goal of the Leading Edge Access Program (LEAP) is to enable university, industry, and government lab access to on-shore state of the art Complementary Metal-Oxide Semiconductor (CMOS) technology for performing advanced integrated circuit (IC) research of benefit to the DoD. Specifically, LEAP offers foundry access at a substantially reduced cost for CMOS technology nodes of 45 nanometers (nm) and below. Currently much of the IC design work performed using advanced technology nodes, including that done for the DoD, uses off-shore facilities in Asia and Europe. This results in substantial intellectual property (IP) development outside the U.S. and creates a number of difficulties for technology transition of DoD-critical applications. This program will stimulate U.S.-based advanced design research, providing top researchers early and partially subsidized access to validate and test innovative ideas and facilitate a more natural transition of these ideas. ***FY 2011 Accomplishments:*** - Completed fabrication and testing of designs at 45 nm Silicon-on-Insulator (SOI) and 32 nm SOI. - Initiated transition discussions to 22 nm bulk CMOS and 22 nm SOI. - Demonstrated over 20 different digital and mixed-signal designs.	3.492	1.000	3.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Held a workshop with potential users highlighting technology capabilities. ***FY 2012 Plans:*** - Develop new foundry offerings in either 22 nanometers or other technologies such as silicon photonics. - Investigate access to alternate semiconductor fabrication facilities. ***FY 2013 Plans:*** - Initiate discussions and develop plans for 14 nanometer and 3D access.			
Title: Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) ***Description:*** The Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) program is developing technology for self-contained chip-scale inertial navigation and precision guidance. This technology promises to effectively mitigate dependence on Global Positioning System (GPS) or any other external signals, and enable uncompromised navigation and guidance capabilities. The program will enable positioning, navigation and timing functions without the need for external information updates by employing on-chip calibration, thereby overcoming vulnerabilities which arise in environments where external updates are not available such as caves, tunnels, or dense urban locations. The technologies developed will enable small, low-power, micro-gyroscopes capable of operating in both moderate and challenging dynamic environments; chip-scale primary atomic clock standards; and on-chip calibration systems for error correction. Advanced micro-fabrication techniques allow a single package containing all the necessary devices (clocks, accelerometers, gyroscopes, and calibration mechanisms) to be incorporated into a volume the size of a sugar cube. The small size, weight and power of these technologies and their integration into a single package responds to the needs of guided munitions, unmanned aerial vehicles (UAVs) and individual soldiers. The successful realization of a Micro PN&T device is dependent on developing fundamentally new batch microfabrication processes, gaining an understanding of the sources and effects of error at the micro-scale, and exploring new combinatorial physics. Innovative 3-D microfabrication techniques will allow co-fabrication of different materials and devices on a single chip. Clocks, gyroscopes, accelerometers, calibration stages, and 3D structures could be integrated into a small, low power architecture. This co-location of different inertial and timing devices opens the possibility for utilization of combinatorial physics in a single micro-system, enabling fast start-up time, increased bandwidth and long-term stability, thus effectively providing very accurate navigation devices. Advanced research for the program is budgeted in PE 0603739E, Project MT-12. ***FY 2011 Accomplishments:*** - Demonstrated 3-D fabrication technique for bubble-blow ULE(TM) glass in a toroidal-shape and silicon micromachined molding process for high Q material hemispheres.	7.963	10.595	16.701

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Explored high aspect ratio etching of fused silica for wafer-scale fabrication and packaging of sensors completely comprised of fused silica. ***FY 2012 Plans:*** - Identify fabrication method to co-fabricate clocks and inertial sensors into a single low power package for navigation microsystems. - Model internal and external sources of error for inertial devices. - Identify self-calibration techniques to compensate for long-term drift. ***FY 2013 Plans:*** - Demonstrate a fabrication technique that allows for the integration of timing and inertial measurement unit into a small package. - Demonstrate the co-fabrication of an inertial sensor and a calibration stage to enable integration of error correction technologies on the same stage. - Use models for internal and external sources of error to develop on-chip calibration algorithms. - Develop an architecture for chip-scale combinatorial atomic navigator. - Demonstrate combinatorial physics for fast startup time, high accuracy inertial devices.			
Title: Advanced X-Ray Integrated Sources (AXIS) ***Description:*** The objective of the Advanced X-Ray Integrated Sources (AXIS) program is to develop tunable mono-energetic X-ray sources that are spatially coherent with greatly reduced size, weight and power while dramatically increasing their electrical efficiency through application of micro-scale engineering technologies such as MEMS and NEMS. Such X-ray sources will enable new versatile imaging modalities based on phase contrast which are 1000X more sensitive than the conventional absorption contrast imaging. Such imaging modalities should enable reverse engineering of integrated circuits to validate trustworthiness as well as battlefield imaging of soft tissues and blood vessel injuries without the injection of a contrast enhancing agent in blunt trauma. It will also reduce radiation dose required for imaging. The Applied Research component of this effort will focus on applying basic research discoveries to the development of compact, pulsed X-ray source. Such sources are a necessary component to enable future technologies with high-speed motion imaging capabilities and the reverse engineering of integrated circuits. This program also includes related basic research efforts funded under PE 0601101E, Project ES-01. ***FY 2012 Plans:*** - Develop advanced designs for compact and energy efficient X-ray sources that are spectrally tunable with narrow energy width. - Develop a coded array of micro-focused X-ray sources for phase contrast imaging. - Design and evaluate the performance potential of a short lifetime photoconductor switched tip-on-post (Spindt) field emitter.	-	4.500	11.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Develop a miniaturized wafer scale electron accelerator and electron storage ring. - Demonstrate the feasibility of an advanced hard x-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and high gain material. ***FY 2013 Plans:*** - Fabricate and demonstrate a short lifetime photoconductor switched tip-on-post (Spindt) field emitter with short pulse duration, high pulse repetition rate and low emittance. - Demonstrate the feasibility of an advanced hard X-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and gain.			
Title: Microscale Plasma Devices (MPD)	-	4.000	9.000
Description: The goal of the Microscale Plasma Devices (MPD) program is to design, develop, and characterize MPD technologies, circuits, and substrates. The MPD program will focus on development of fast, small, reliable, carrier dense, microplasma switches capable of operating in extreme conditions such as high-radiation and high-temperature environments. Specific focus will be given to methods that produce efficient, high-pressure (up to or even beyond atmospheric pressure) generation of ions, radio frequency energy, and light sources. Applications for such devices are far reaching, including the construction of complete high-frequency plasma-based logic circuits, and integrated circuits with superior resistance to radiation and extreme temperature environments. It is envisaged that both two and multi-terminal devices consisting of various architectures will be developed and optimized under the scope of this program. MPDs will be developed in various circuits and substrates to demonstrate the efficacy of different unique approaches. The MPD applied research program is focused on transferring the fundamental scientific advances funded by PE 0601101E, Project ES-01 to produce complex circuit designs that may be integrated with commercial electronic devices. It is expected that the MPD program will result in the design and modeling tools, as well as the fabrication capabilities necessary to commercially manufacture high-performance microscale plasma device based electronic systems for advanced DoD applications. ***FY 2012 Plans:*** - Complete definition of complex circuit demonstrations of DoD relevant high-performance microplasma electronics. - Develop microplasma simulation design tools (MSDT) for commercial integration of optimized microplasma electronics with commercial electronic devices. - Design and develop a complete set of microplasma electronics capable of producing a complete radiation hardened RF system. - Develop a microcavity material capable of passively protecting against high power microwave pulses. ***FY 2013 Plans:*** - Optimize microplasma simulation design tool (MSDT) for commercial development of microplasma based electronics.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Begin construction of a full microplasma electronics based radiation hardened RF system. - Initial testing of a microcavity material for high power microwave protection.			
Title: IntraChip Enhanced Cooling (ICECool) ***Description:*** The IntraChip Enhanced Cooling (ICECool) program is exploring disruptive technologies that will remove thermal barriers to the operation of military electronic systems, while significantly reducing size, weight, and power consumption. These thermal barriers will be removed by integrating thermal management into the chip, substrate, or package technology. Successful completion of this program will close the gap between chip-level heat generation density and system-level heat removal density in RF arrays and embedded computers. Specific areas of focus in this program include overcoming limiting evaporative and diffusive thermal transport mechanisms at the micro/nano scale to provide an order-of-magnitude increase in on-chip heat flux and heat removal density, determining the feasibility of exploiting these mechanisms for intrachip thermal management, characterizing the performance limits and physics-of-failure of high heat density, intrachip cooling technologies, and integrating chip-level thermal management techniques into prototype high power electronics in the form factor of RF arrays and embedded computing systems. ***FY 2013 Plans:*** - Investigate advanced evaporative, thermoelectric, and diffusive technologies for intrachip thermal management in electronic and photonic components. - Determine fundamental limits of advanced thermal technologies and feasibility of implementation into compact defense electronic and photonic systems. - Investigate benefits to system-level performance and size, weight, power, and cost (SWaPC) through the use of intrachip thermal management technologies.	-	-	8.000
Title: In vivo Nanoplatforms (IVN) ***Description:*** The In vivo Nanoplatforms (IVN) program seeks to develop the nanoscale systems necessary for in vivo sensing and physiologic monitoring and delivery vehicles for targeted biological therapeutics. The nanoscale components to be developed will enable continuous in vivo monitoring of both small (e.g. glucose, lactate, and urea) and large molecules (e.g. biological threat agents). A reprogrammable therapeutic platform will enable tailored therapeutic delivery to specific areas of the body (e.g. cells, tissue, compartments) in response to traditional, emergent, and engineered threats. The key challenges to developing these systems include safety, toxicity, biocompatibility, sensitivity, response, and targeted delivery. The IVN program will have diagnostic and therapeutic goals that enable a versatile, rapidly adaptable system to provide operational support to the warfighter in any location.	-	-	5.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
FY 2013 Plans: - Begin development of initial in vivo diagnostic platform for small molecules. - Initiate development of in vivo therapeutic platform for treatment of infectious disease. - Begin technical analysis of safety and efficacy for proposed in vivo platforms.			
Title: Pixel Network (PIXNET) for Dynamic Visualization ***Description:*** The Pixel Network (PIXNET) for Dynamic Visualization program aims to develop infrared imaging components and the necessary application programming interface (API) system to provide real-time and dynamic tactical visualization of battlefield situation awareness and exploitation at individual level and at collective ensemble. The goal is to enable one-to-many and many-to-one real-time intelligence, surveillance and reconnaissance (ISR) data and metadata to maximize mission relevancy and minimize decision time during day/night operations. The program will focus on significant reduction in cost, size, weight and power (SWaP) of infrared sensor components to enable portability and ability to deploy widely to all participants in the theatre. Development of wafer scale IR sensor and coolers for low cost manufacturing will provide a price point that will allow them to be deployed to each warfighter. The emphasis on a small form -factor (<3.5 cm3) will naturally enable new opportunities such as surveillance with micro-UAVs, networked handheld devices with fused imaging capabilities to share tactical information at troop level, and intelligence for rapid decision/action. The phenomenology of different infrared wavelengths will be exploited for targets of interest and only relevant data will be transmitted, thus reducing data burden over the network. Having the capability of PIXNET at the soldier level will increase situational awareness and will enable more effective tactics, techniques and procedures (TTP). PIXNET will take advantage of small computing platforms such as Android cell phones API to integrate and demonstrate digital image data distribution and signal processing via wireless connectivity. The Program Executive Office, Space Sciences Laboratory, PM Optics USMC and industry will be the transition partners. ***FY 2013 Plans:*** - Develop and review IR camera design and overall architecture that will demonstrate digital image data distribution and signal processing via wireless connectivity using a cell phone or PDA platform. - Develop CMOS compatible wafer scale manufacturing of integrated image sensor-cooler for very low SWaP IR camera technology. - Develop wafer scale low-cost and high transmission optics. - Develop strategy to reduce IR image sensor cost by 15 to 50X. - Demonstrate rudimentary operation of networked IR sensors for digital signal processing and image data distribution.	-	-	12.000
Title: Microscale Power Conversion (MPC)	15.000	-	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
Description: The Microscale Power Conversion (MPC) program will address the fundamental limitations of power conversion by enabling a new technology and approach that exploits advances in basic power devices that can operate at very high frequencies with low losses. A key benefit of these new devices is that they can be integrated into very compact circuits and assemblies that will provide dramatic advances to the power bus of a platform. Specifically, this program will develop the technology to enable DC to DC power conversion for military applications at the scale of an integrated circuit so it can be embedded within the electronics subsystem and a new distributed power architecture can be realized. The focus of this program is on attaining 100MHz internal operation frequencies of power circuits since the size of the passive elements (inductors and capacitors) in a power converter scales inversely as the fourth power of the internal operating frequency. In FY 2012, MPC moves to PE 0602715E, Project MBT-03. ***FY 2011 Accomplishments:*** - Initiated design and initial fabrication of critical sub-circuits and performed measurements in laboratory in order to design and prototype amplifier architectures for highly efficient handling of large peak-to-average ratio RF waveforms for military systems. - Initiated development of theoretical design and analyses to understand the high-frequency trade-off space of relevant circuit designs and topologies. - Initiated co-design of advanced X-band power amplifier technologies to include drain and gate bias modulation, dynamic output impedance matching, and closed-loop control to enable fast switching power modulation. - Optimized transistor performance to include ultra-fast power switching capability. - Initiated development of very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers. - Developed new fabrication techniques for incorporating high frequency transistors and devices compatible with integrated power amplifier topologies.			
Title: Carbon Electronics for RF Applications (CERA) ***Description:*** The Carbon Electronics for RF Applications (CERA) program developed a wafer-scale graphene (2-D carbon monolayer) synthesis process resulting in films with excellent mobility, uniformity and layer control (down to single monolayer films). These carbon films will be used to develop ultra-low power, high-speed field effect transistors optimized for RF-applications (RF-FET). The program concluded with a demonstration of a low power, low noise amplifier (LNA) using graphene-field effect transistors (FETs) as the channel material. ***FY 2011 Accomplishments:*** - Optimized synthesis process for wafer-scale graphene thin films. - Optimized RF-FETs based on graphene channels. - Increased area of graphene synthesis to wafer-scale dimensions.	6.958	-	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Demonstrated film thickness control down to single monolayers and bi-layers. - Demonstrated low power, high performance RF-FETs with graphene. - Demonstrated initial graphene channel based RF-FETs in mixer circuits.			
Title: Quantum Sensors ***Description:*** The Quantum Sensors program exploited non-classical effects to improve the resolution and range of military sensors. The objective of the program was to enhance sensitivity, resolution, and effectiveness of electromagnetic sensors beyond what is classically possible. In the initial effort, the types of sensors that propagate entangled light out to and back from a target were proven to be ineffective when realistic scattering and absorption occur between the source and the target. Sensors that propagate classical light to the target but use non-classical effects only in the receiver were shown to provide qualitative advantages over their classical counterparts. These include compensation for soft aperture losses using squeezed vacuum injection and compensation for detectors' quantum inefficiency using noiseless amplification. ***FY 2011 Accomplishments:*** - Tested and demonstrated system performance. - Made technology available to the Services for further development.	5.389	-	-
Title: Spin Torque Transfer-Random Access Memory (STT-RAM) ***Description:*** The Spin Torque Transfer-Random Access Memory (STT-RAM) program developed materials and processes to fully exploit the spin-torque transfer (STT) phenomenon for creating "universal" memory elements. This program developed the core technology for exploiting spin-torque transfer and related phenomena for producing large-scale non-volatile memories. Compatibility and stability with expected mainstream processes for semiconductor electronics and patterned media is an important attribute that should enable significant leverage for these new technologies in delivering early demonstrations and in gaining wider acceptance. ***FY 2011 Accomplishments:*** - Demonstrated improved magnetic materials and non-volatile memory bits, in the STT architecture, with 100x faster speed and 1000x lower power for switching than flash memory. - Demonstrated manufacturing processes that produce fast low power STT memory arrays in high yield.	4.565	-	-
Title: Radio Frequency Photonics Technology (RPT) ***Description:*** The Radio Frequency Photonics Technology (RPT) program developed components and microsystems to revolutionize deployed signal intelligence (SIGINT) gathering capabilities. The radio frequency (RF) spectrum contains innumerable friendly and adversarial signals of interest including: voice and data communications, electronic signatures, and navigation information. Conventional electronic systems are challenged in detecting weak signals in the presence of strong	16.929	-	-

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APPROPRIATION/BUDGET ACTIVITY 0400: *Research, Development, Test & Evaluation, Defense-Wide* BA 2: *Applied Research*	**R-1 ITEM NOMENCLATURE** PE 0602716E: *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
ones (low-linearity) across a broad range of frequencies (narrow-band). The RPT program aimed to efficiently capture all RF signals of interest by developing broad-band (>10 gigahertz) high-linearity (>70 decibels dynamic-range) optical components and microsystems. RPT enables linear broadband microsystems such as remote links, channelizers, and analog-to-digital converters (ADCs). The RPT program will reduce susceptibility to electronic attack, increase the probability-of-intercepting (POI) adversaries on their first-pulse transmission, and increase information awareness 1000-fold. ***FY 2011 Accomplishments:*** - Developed on-chip integrated optical waveguides with loss of less than 0.1dB/m using two different approaches based on silicon dioxide-core and silicon nitride-core waveguides. This enables 100 ns of delay on a chip. - Developed an analog to digital converter performance multiplier architecture that enables a 3 bit enhancement to electronic ADCs.			
Title: Ultrabeam ***Description:*** The goal of the Ultrabeam program was to demonstrate the world's first gamma-ray laser using laboratory equipment. Compact gamma ray lasers can enable the development of new and more effective radiation therapies and radiation diagnostic tools for medical and materials/device inspection applications. This unique X-ray laser technology could also eventually enable the development of compact, laboratory-scale high-brightness coherent sources for 3-D molecular scale imaging of living cells and debris-free advanced lithography. ***FY 2011 Accomplishments:*** - Demonstrated stable consistent operation of an Xe(L,M) X-ray with indirect evidence for inferred pulse energies of 10's megajoules (mJ) and pulse durations as short as 10's of attoseconds. - Modeled gamma-ray gain of >100 per cm at ~100 kilo electron volt (keV) photon energy.	1.846	-	-
Title: Chip-to-Chip Optical Interconnects (C2OI) ***Description:*** The performance of electronic interconnect technologies, particularly for implementing high-speed communications channels on printed circuit boards and back planes, is currently being outpaced by the ever-advancing needs of complementary metal-oxide semiconductor (CMOS) microprocessor chips. This performance gap in the on-chip and between chip interconnection technology will create substantial data throughput bottlenecks, deleteriously affecting future military-critical sensor signal processing systems. To address this pressing issue, the Chip-to-Chip Optical Interconnects (C2OI) program developed optical technology for implementing chip-to-chip interconnects at the board and backplane level. ***FY 2011 Accomplishments:*** - Demonstrated a chip-scale, opt-electronic transceiver circuit based on C2OI technology operating at 1 terabit per second (consisting of twenty-four bidirectional channels each operating at 20 gigabits/second).	1.322	-	-

Exhibit R-2, RDT&E Budget Item Justification: PB 2013 Defense Advanced Research Projects Agency	DATE: February 2012
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C. Accomplishments/Planned Programs ($ in Millions)	FY 2011	FY 2012	FY 2013
- Demonstrated the integration of C2OI opt-electronic transceiver technology with commercially fabricated circuit boards by demonstrating fully operational data channels operating at 15 gigabits/second link.			
Title: Near-Junction Transport (NJTT) ***Description:*** Miniaturization and integration in microelectronics have led to a thermal bottleneck where dense logic circuits, mixed-signal analog and digital circuits, and RF electronics are all limited by energy dissipation in the small volumes adjacent to the electronically-active junctions. The Near-Junction Thermal Transport (NJTT) program explored heat conduction and hot spot mitigation through the materials layers near a high-power device junction. This program concentrated on development of specific materials and substrate bonding techniques, as well as microfluidic cooling, to enhance dissipated heat removal in the region of the active junctions of semiconductor chips. Attention was also devoted to development and verification of metrology and quantitative models for heat generation and transport in and near device junctions. Industry leaders with the expertise in developing high-power semiconductor devices are expected to demonstrate devices with significantly enhanced heat density and consequent enhancement in performance metrics. This program was a companion program to the Thermal Management Technologies (TMT) program in PE 0603739E, Project MT-12. ***FY 2011 Accomplishments:*** - Developed techniques for utilizing high conductivity substrates and liquid cooling for use in high power GaN electronics. - Designed GaN electronics that provided improved output power through improved near junction thermal management.	7.089	-	-
Accomplishments/Planned Programs Subtotals	256.631	215.178	222.416

D. Other Program Funding Summary ($ in Millions)

N/A

E. Acquisition Strategy

N/A

F. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.